A D-Band Monolithic Fundamental Oscillator Using InP-Based HEMT's

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Abstract—**The design, analysis, and experimental characteristics of the first fundamental D-band monolithic HEMT oscillator are reported. The circuit is based on a dual feedback topology and uses 0.1 μm pseudomorphic double heterojunction InAlAs/$In_{0.7}Ga_{0.3}As$ HEMT's. It includes on-chip bias circuitry and an integrated E-field probe for direct radiation into the waveguide. The circuit was analyzed using both small-signal and large-signal methods, while carefully accounting for the high-frequency effects of the InP-based HEMT's. An oscillation frequency of 130.7 GHz was measured and the output power level was −7.9 dBm using HEMT's of small gate periphery (90 μm). The measured power characteristics were compared to the simulation and yielded good agreement. This represents the highest frequency of fundamental signal generation out of monolithic chips using three-terminal devices.**

I. Introduction

LATTICE-MATCHED and strained (pseudomorphic) InAlAs/InGaAs HEMT's on InP substrates are recognized as the most suitable components for operation at millimeter-wave frequencies. Discrete devices have demonstrated a high f_{max} of 455 GHz [1] and an f_T of 340 GHz [2]. Psuedomorphic InAlAs/$In_xGa_{1-x}As$ ($x > 0.53$) HEMT's are particularly promising candidates for high-frequency and low-noise applications due to the superior material properties of the strained InGaAs channel. The strained InGaAs channel has larger Γ-to-L valley separation, and thus offers higher peak and average velocities compared to lattice matched channels. Pseudomorphic devices may, however, face problems of poor output conductance and limited power performance. These problems can be alleviated by employing a double heterostructure (DH) design. The bottom heterojunction helps to improve carrier confinement and increases the electron density in the channel. As a result, DH-HEMT's show high f_{max} and larger current densities, and are therefore very promising for high-frequency oscillator applications [3].

Monolithic microwave circuits have so far been using primarily GaAs-based devices such as MESFET's or HEMT's. As far as the high-frequency monolithic oscillators are concerned, GaAs-MESFET's and AlGaAs/InGaAs HEMT's have been used as signal sources up to W-band and slightly above [4], [5]. High-frequency monolithic circuits using InP-based HEMT's have started emerging recently and include ultrabroadband amplifiers [6] and W-band mixers [7]. InP-based HEMT's have also been used for the realization of monolithic oscillators. Ka-band oscillators were investigated by the authors and showed a record high DC-to-RF efficiency of 36 percent at 35 GHz [8] and W-band oscillators operated around 80 GHz with an output power of 1.2 mW using 36 μm gate periphery devices [9]. Various applications such as, for example, space-based remote sensing and radiometry require signal generation above 100 GHz. A fully integrated D-band oscillator-doubler chain has been developed for this purpose, demonstrating an output power of −12 dBm at 132 GHz [10]. Fundamental sources are, however, a preferred solution compared to frequency multiplication techniques. Since GaAs-based devices may be limited from being used at frequencies well above 100 GHz due to their modest f_{max} and gain, InP-based HEMT's are of prime interest for monolithic fundamental oscillator applications at these frequencies.

In this work, the design, fabrication, and performance of a D-band monolithic fundamental oscillator are presented, together with a small- and large-signal analysis which carefully accounts for the high-frequency and nonlinear effects of the InP-based HEMT's. The monolithic oscillator uses a 0.1 μm × 90 μm pseudomorphic double heterojunction InAlAs/InGaAs/InAlAs HEMT. The circuit operates at 130.7 GHz with an output power of −7.9 dBm. This is the first demonstration of the fundamental signal generation at 130 GHz out of a monolithic chip using three-terminal devices. Section II describes the MMIC fabrication steps and dc and microwave characteristics of 0.1 μm pseudomorphic DH InAlAs/$In_{0.7}Ga_{0.3}As$ HEMT's used in the oscillator circuit. The circuit design and small- and large-signal analysis are presented in Section III. Finally, measured oscillator characteristics are compared to the calculated data in Section IV.

II. Device Characteristics and MMIC Fabrication

The layer structure of InAlAs/InGaAs HEMT's used in this work is shown in Fig. 1. The HEMT's are based on the double heterojunction design (DH) and employ a

Manuscript received April 5, 1993; revised July 1, 1993. This work was supported by URI under Contract DAAL 03-92-G-0109 and by NASA under Contract NAGW-1334.

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IEEE Log Number 9212951.

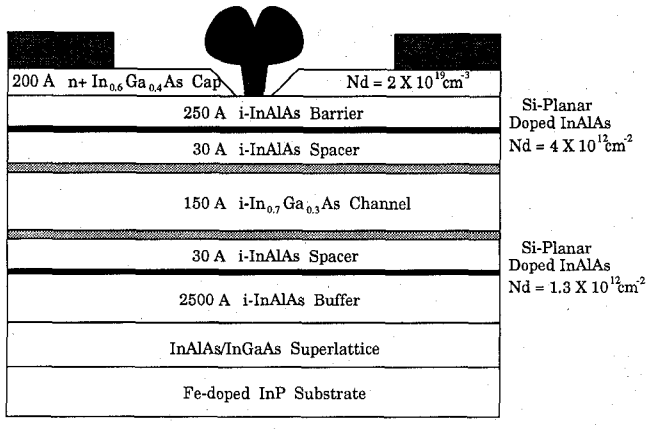

Fig. 1. Layer structure of the pseudomorphic double heterostructure InAlAs/InGaAs HEMT's.

strained $In_{0.7}Ga_{0.3}As$ channel. The wafer was grown on a semi-insulating InP substrate by MBE at TRW. The structure consists of: 1) a 200 Å indium-rich $In_{0.6}Ga_{0.4}As$ cap layer, heavily doped with Si ($2 \times 10^{19}/cm^3$), for low resistivity ohmic constants; 2) a 250 Å undoped InAlAs Schottky barrier layer; 3) a top Si-planar doped donor layer with a doping density of $4 \times 10^{12}/cm^2$; 4) a 30 Å spacer layer; 5) an undoped strained $In_{0.7}Ga_{0.3}As$ channel; 6) another 30 Å spacer layer; 7) an additional bottom planar doped layer with a lower doping density ($1.3 \times 10^{12}/cm^2$); and 8) a 2500 Å undoped InAlAs buffer. The 2DEG is formed both at the top InAlAs/InGaAs and the bottom InGaAs/InAlAs heterojunction. The $In_{0.7}Ga_{0.3}As$ channel with 17 percent excess indium offers better carrier transport and improved confinement than lattice-matched designs. The bottom heterojunction of DH-HEMT's allows them to have a low output conductance and large current density, which leads to high f_{max} and large power density, respectively. DH-HEMT's are therefore very promising for oscillator applications. The Hall mobility of the layers used in this work was about 9000 $cm^2/V \cdot s$ and the carrier concentration was $4.5 \times 10^{12}/cm^2$ at room temperature.

The D-band monolithic circuits were fabricated using the InP-based MMIC process developed at the University of Michigan. Optical lithography was used for all the steps except for the 0.1 μm gate definition where E-beam lithography was employed. First, mesas were defined by chemical etching using an H_3PO_4-based solution. Ohmic contacts were formed by depositing Ge/Au/Ni/Ti/Au (700/1400/500/200/1000 Å) and followed by rapid-thermal annealing at 375°C for 7 s. The ohmic contact resistivity was around 0.15 $\Omega \cdot$ mm. The JEOL JBX 5DIIF E-beam lithography system was used to define 0.1-μm-long mushroom-shaped gates. Two line scans with different doses were used for this purpose. The gate recess etching was performed by wet chemical etching and Ti/Pt/Au was deposited as gate metal. The overlay capacitors were realized by lifting off sputtered SiO_2. Interconnects and microstrip elements were realized using evaporated thick Ti/Au (1000/10 000 Å). Airbridges were finally formed by electroplated Au.

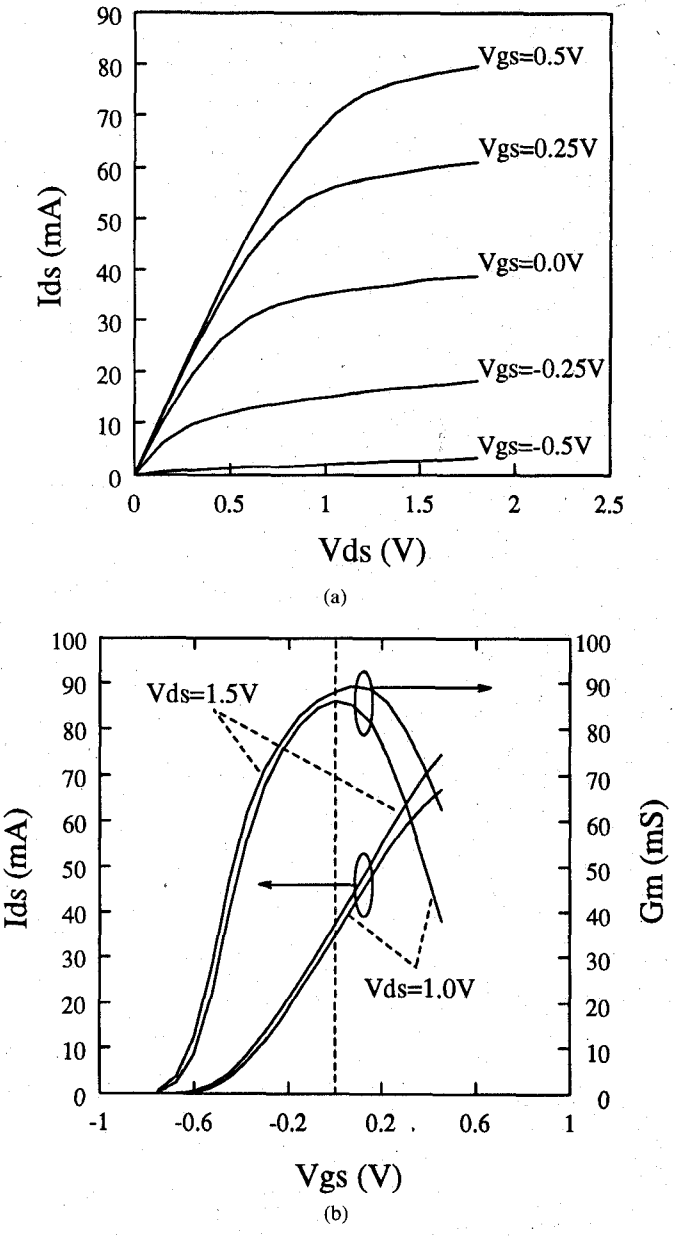

Fig. 2. The dc I-V characteristics of a typical double heterojunction InAlAs/InGaAs HEMT (L_g = 0.1μm, W_g = 90 μm): (a) I_{ds} versus V_{ds}, and (b) I_{ds} and G_m versus V_{gs}.

The dc characteristics of a typical 0.1 μm × 90 μm DH-HEMT are shown in Fig. 2(a) and (b). The devices showed an extrinsic dc transconductance of 1000 mS/mm and a maximum current density close to 1 A/mm. The source-to-drain breakdown voltage was limited to about 2 V for this pseudomorphic design, and excellent pinchoff characteristics were found. The I-V characteristics do not reveal the presence of "kink" effect—an effect often observed in pseudomorphic single heterojunction HEMT's due to trapping and detrapping of carriers injected into the InAlAs buffer. The additional bottom heterojunction in the DH design employed in this work apparently serves as a barrier and prevents the carriers from being injected into the buffer layer, resulting in "kink"-free I-V characteristics and reduced output conductance. The dc output conductance was as low as 46.7 mS/mm and the dc volt-

age gain (G_m/G_{ds}) was about 21.4. The dc transfer characteristics in Fig. 2(b) do not show multiple peaks in G_m versus V_{gs} curve, which is attributed to the small InGaAs channel thickness (150 Å); two 2DEG's are placed so closely together that the overlap between them is dominant. On-wafer probing was performed at the end of the whole MMIC process to evaluate high-frequency characteristics of the devices, and an extrinsic f_T of 140 GHz and an f_{max} of 270 GHz were found.

III. Monolithic Oscillator Design and Analysis

The oscillator analysis of this work was based on both small-signal and large-signal HEMT models. Small-signal parameters can be used to check the criteria of oscillation startup and give fairly accurate estimation of the oscillation frequency, as will be shown later on in this section. However, large-signal modeling is required to analyze nonlinear properties and accurately estimate the output power level of the oscillators.

Modeling of oscillators at frequencies above 100 GHz faces special difficulties. Small parasitic capacitances and inductances, which have very little effect at low frequencies, may play an important role and change the oscillation conditions. Accurate active device modeling is also very difficult due to lack of vector measurement tools at these frequencies. HEMT modeling therefore has to rely on the S-parameter data measured at low frequencies. In this case, the equivalent circuit elements extracted from low-frequency S-parameters are used to predict the properties of the device at high frequencies. This assumes validity of the equivalent circuit and invariance of the circuit element values over the frequency range of several octaves. To improve the simulation accuracy, the small-signal and large-signal analysis reported in this paper were done by carefully accounting for the high-frequency effects present in D-band operated InP-HEMT's.

A. Small-Signal Analysis

S-parameters of the HEMT's were measured from 1 to 26 GHz using on-wafer probing at various bias points. Equivalent circuit elements were then extracted from measured multibias S-parameters using an analytical approach similar to that discussed in [11] and [12], but modified to account for the special properties of short-gate length InP-HEMT's. The equivalent circuit topology and element values at one bias point are shown in Fig. 3. Separate "cold" measurements were performed to evaluate the bias independent extrinsic elements such as series resistances, inductances, and pad capacitances. Intrinsic Y-parameters (Y_i) were calculated at each frequency from the measured S-parameters by stripping off the effects of the external elements. The bias-dependent intrinsic elements, which were expressed as analytic functions of Y_i's, could then be evaluated by averaging the data obtained at all measurement frequencies. This method allows good estimation of the intrinsic elements, except for R_i and τ, which sometimes turn out to be negative and show large

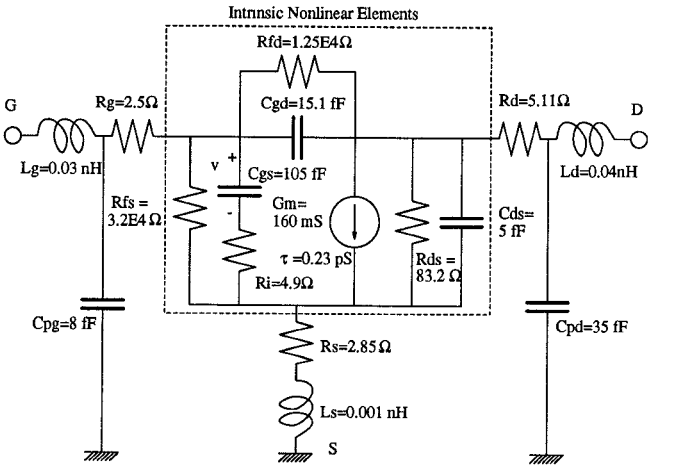

Fig. 3. Equivalent circuit of HEMT's (V_{gs} at maximum G_m condition and V_{ds} = 1.1 V).

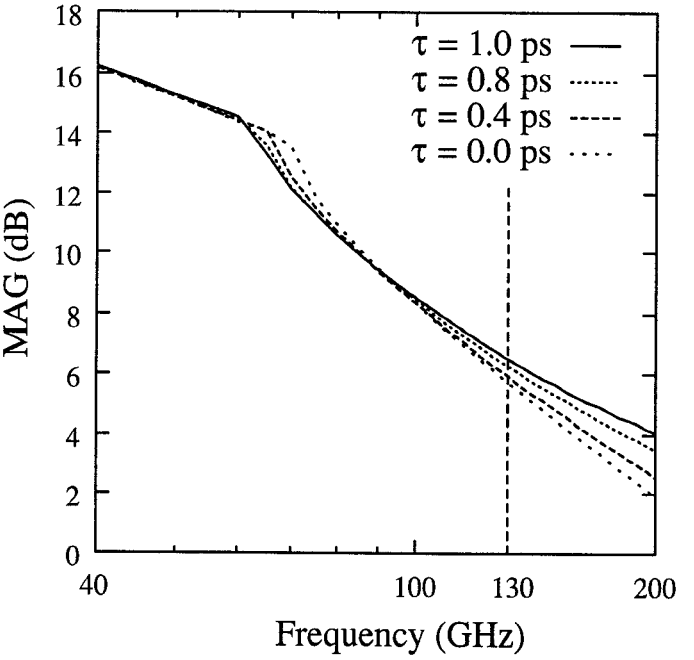

Fig. 4. Maximum available gain as a function of frequency for various τ's.

frequency dispersion in submicron InP-based HEMT's. These elements are usually small in magnitude for short-gate length devices and have little effect on device performance, and thus S-parameters at low frequencies. Their impact on high-frequency characteristics can, however, be significant.

The impact of τ on the device performance at high frequencies is demonstrated in Fig. 4. The maximum available gain (MAG) is plotted here as a function of frequency for various τ's. The measured device has an estimated f_{max} of 270 GHz and MAG was about 6 dB at 130 GHz. The low-frequency gain is almost unaffected by the choice of τ and from 60 to 90 GHz, the MAG becomes smaller as τ increases. However, the opposite trend is found at frequencies higher than 90 GHz, i.e., as τ is increased, the MAG becomes larger. Even if the gain variation with τ may be limited to at most 1 dB, this effect

cannot be ignored since the power gain itself is also small at these frequencies. Inaccurate τ extraction may, in particular, lead to significant errors in calculating the negative resistance and estimating the oscillation power.

In view of the above difficulties, the following extraction method has been used in order to evaluate R_i and τ accurately. As shown later, accurate extraction of τ is not possible without knowing the correct value of R_i. Hence, the R_i extraction is discussed first. From Fig. 3, the real part of the sum of $Y_{i,11}$ and $Y_{i,12}$ can be written as

$$\text{Re}\,[Y_{i,11} + Y_{i,12}] - g_{fs} = \frac{\omega^2 R_i C_{gs}^2}{1 + \omega^2 R_i^2 C_{gs}^2} \quad (1)$$

where g_{fs} is equal to $1/R_{fs}$. The ω^2 term of the above equation makes the magnitude of the right-hand side (RHS) term very small at low frequencies. In fact, this term becomes so small that it is often comparable to the noise level of the measurement. To reduce the ω^2-effect, it is therefore advisable to use only high-frequency Y-parameter data in extracting R_i. Equation (1) can be rearranged for this purpose as follows:

$$RZ_{i,1} \equiv \frac{1}{\text{Re}\,[Y_{i,11} + Y_{i,12}] - g_{fs}} = R_i + \frac{1}{R_i} \cdot \frac{1}{C_{gs}^2 \omega^2}. \quad (2)$$

Based on this equation, it is obvious that plotting $RZ_{i,1}$ against $1/(\omega C_{gs})^2$ gives R_i by the zero intercept and $1/R_i$ by the slope. The use of this equation in the HEMT's of this work showed that the magnitude of $RZ_{i,1}$ and the second term in the RHS are very large—more than 1 kΩ at 26 GHz for HEMT's biased at maximum G_m. Therefore, extracting a small value of R_i from the zero intercept point of $RZ_{i,1}$ versus $1/(\omega C_{gs})^2$ can be quite erroneous. The slope of the plot at high frequencies can, on the other hand, result in a good estimation of R_i, as illustrated in Fig. 5. The curve corresponding to (2) was plotted here for two different V_{gs} bias points. The results show that R_i is higher at more negative V_{gs} bias (toward pinchoff of the device), as expected from the theory, due to the smaller number of carriers in the channel.

Having evaluated R_i, τ can be extracted as follows. From the intrinsic equivalent circuit of Fig. 3, one finds

$$Y_{i,21} - Y_{i,12} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_g s}. \quad (3)$$

The equation for the angle of the complex variables of (3) can be written as

$$\alpha \equiv \text{Ang}\,(Y_{i,21} - Y_{i,12}) + \arctan\,(\omega R_i C_{gs}) = -\omega\tau \quad (4)$$

where Ang(Y) denotes the angle of the complex variable Y ($= Y_{i,21} - Y_{i,12}$). The relationship between the left-hand side (LHS) of (4) and angular frequency (ω) turns out to be linear. Furthermore, the slope of the linear relationship can be used to determine τ. In order for this extraction to be meaningful, R_i should be known accurately, otherwise, the errors in the second term of the LHS of (4) dominate and make a meaningful extraction of τ impossible. R_i's evaluated from the previous method were used to find out the τ of the HEMT, and the results are shown in Fig. 6 for two V_{ds} bias points. It is found that τ is larger for higher V_{ds}. Since τ is associated with the transit time in the velocity-saturated region toward the drain side of the gate, it is reasonable to observe such a trend.

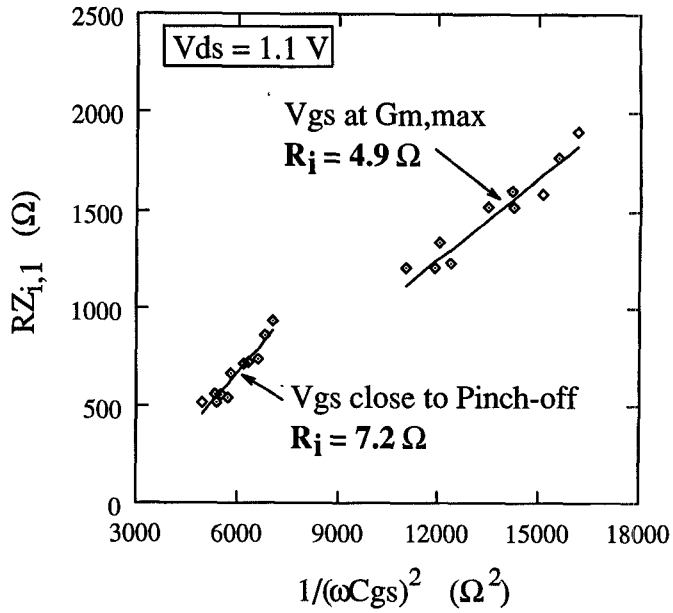

Fig. 5. R_i extraction from the slope of $RZ_{i,1}$ versus $1/(\omega C_{gs})^2$ at two different V_{gs} points.

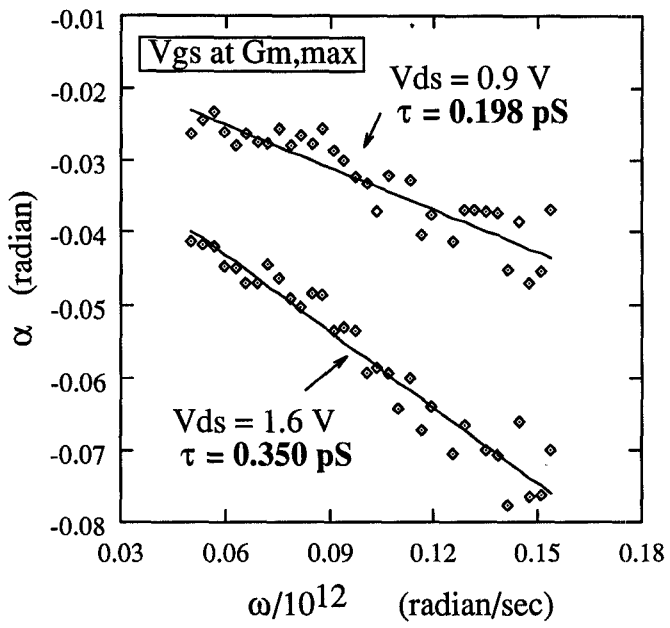

Fig. 6. τ extraction from the slope of α versus ω at two different V_{ds} points.

B. Oscillator Design

The oscillator was first designed based on small-signal analysis which employed the HEMT equivalent circuit derived using the extraction technique described in Subsection A. The load impedance was then determined using

a large-signal analysis technique. The equivalent circuit schematic of the D-band monolithic oscillator is shown in Fig. 7. The oscillator uses a common source HEMT configuration with a dual feedback scheme consisting of a series feedback element from source to ground and a parallel feedback element from drain to gate. The feedback elements were designed to maximize the negative resistance at the drain of the HEMT. The overall gain of this oscillator circuit is limited to a small value due to the small gain of the HEMT's in the frequency range of operation and the mismatches and losses introduced by the passive elements such as the feedback loops and source grounding. Compared to the single series feedback, the dual feedback topology permits us, however, to obtain higher negative resistance over narrower frequency range. It also has the potential of providing larger output power, as already demonstrated at Ka-band [8].

The series feedback is realized with a high impedance transmission line. For the parallel feedback, a voltage transforming element realized with a combination of phase delay lines and edge-coupled lines is used. The edge-coupled lines are used for dc blocking instead of MIM capacitors due to the high loss of the latter at frequencies above 100 GHz. Microstrip stubs are used at the output for impedance transformation in order to provide the optimum termination conditions at the drain terminal. The termination condition was evaluated using a large-signal simulation method described elsewhere [13]. The open-ended line on the gate side of the device is designed to determine the oscillation frequency.

The D-band output signal was directly radiated into a WR-5 waveguide using a monolithically integrated on-chip E-field probe. The probe was designed based on scaling from low-frequency data. No external microstrip-to-waveguide transition was therefore needed, and bonding was avoided on the RF side of the chip. The biasing circuitry consisting of a quarter-wavelength line and a radial stub was also integrated on the chip. Stabilization circuits were incorporated both on-chip and off-chip to suppress undesirable parasitic oscillation at low frequencies. An on-chip 50 Ω series resistor realized with thin titanium film was added to the gate side, and an off-chip capacitor and 50 Ω resistor were used in the drain bias terminal for circuit stabilization.

C. Large-Signal Oscillator Analysis

A large-signal oscillator analysis was performed to investigate the nonlinear properties of the oscillator circuit at high frequencies and to predict the output power level. For this purpose, the oscillator circuit is partitioned into an active and a passive circuit. The latter represents either a load or a resonator. The steady-state oscillation condition can then be written as follows [14]:

$$\Gamma_a(\omega, P) \cdot \Gamma_p(\omega) = 1 \qquad (5)$$

where Γ_a and Γ_p denote the one-port reflection coefficient of the active and passive subcircuit, respectively. Γ_a is a function of both the angular frequency (ω) and power (P)

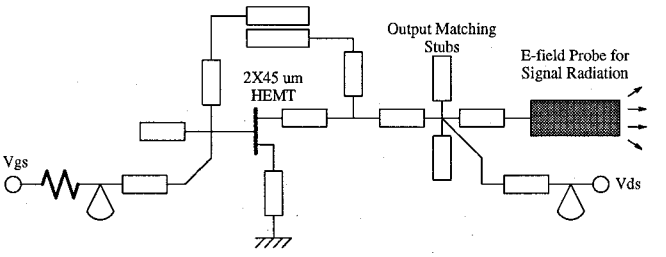

Fig. 7. Equivalent circuit schematic of the dual feedback D-band oscillator.

into the active device. As the oscillation builds up from noise, the oscillation power increases and the magnitude of Γ_a decreases until the steady-state oscillation condition of (5) is satisfied. In the computer-aided analysis of this work, the two variables, P and ω, were varied until a solution was found for the above equation. The oscillation power was then calculated from the power delivered to the load under this steady-state oscillation condition.

The accuracy of the oscillator analysis depends largely on that of the nonlinear active device modeling. The nonlinear models of the HEMT's used here were based on multibias small-signal equivalent circuits discussed earlier. The extracted multibias small-signal elements were used to construct a large-signal model using a 2-D cubic spline technique, as described in [7] and [9]. This method has two major advantages when it is applied to the nonlinear analysis of high-frequency InP-based HEMT's: 1) it does not rely on dc parameters which may be quite different from the high-frequency values due to frequency dispersion characteristics of HEMT's; 2) compared to the method using predefined bias-dependent formulas with curve-fitting parameters, it has the least interpolation errors. This approach is, consequently, most suitable for modeling highly nonlinear devices, such as the InP-HEMT's of this work. The nonlinear current and charge at each node were evaluated by integrating the voltage-dependent conductance and capacitance with respect to the gate and drain voltages [15], [16]. These were then subsequently used in harmonic balance routine for analyzing the circuit. The validity of the model has been verified by comparing the measured S-parameters to the simulated ones which have been calculated as the ratio of reflected (or transmitted) and incident waves under small-signal single-tone excitation. The latter corresponds, of course, to "large-signal-type" S-parameters under limit conditions of small power level operation. The results of this comparison are shown in Fig. 8. Very good agreement is found between them over the entire measurement frequency range. The model has also been validated using load-pull measurements, as demonstrated in [13].

The monolithic D-band oscillator was simulated using the large-signal analysis method with V_{gs} biased at the maximum g_m point ($V_{gs} = -0.1$ V) and V_{ds} at 1.3 V. The simulated oscillation frequency was around 135.2 GHz with an output power level of -5 dBm. The oscillation frequency change with the power level has been calculated to investigate the difference between small-signal

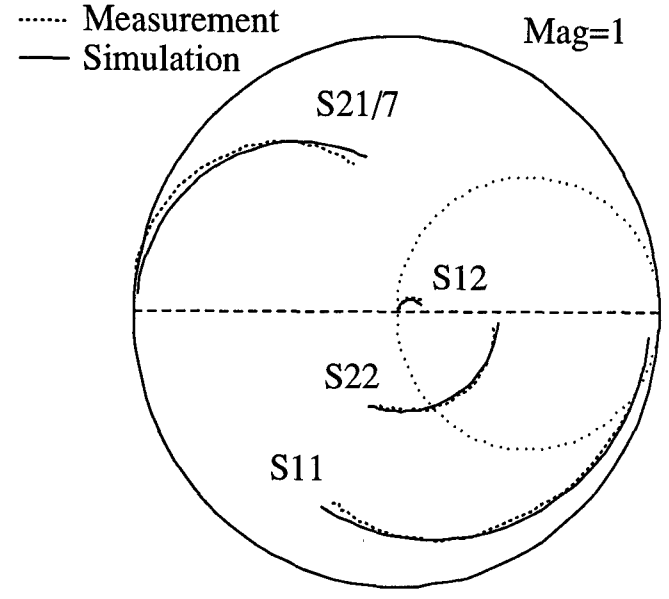

Fig. 8. Comparison between measured and simulated *S*-parameter. Frequency is swept from 1 to 26 GHz. Simulated *S*-parameters are calculated using the nonlinear model of HEMT and harmonic balance analysis under the small-signal single-tone excitation.

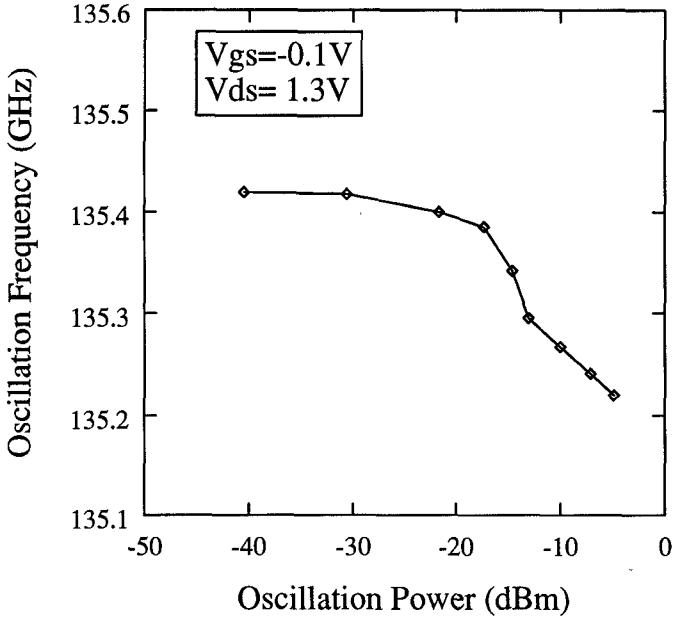

Fig. 9. Simulated oscillation frequency dependence on the oscillation power at the load.

and large-signal oscillation conditions in terms of frequency. Fig. 9 shows the frequency at which the sum of the angles of $\Gamma_a(\omega, P)$ and $\Gamma_p(\omega)$ equals zero as the power into the device (P) increases from small signal to the steady-state oscillation signal; the X-axis actually represents the oscillation power at the load which is, of course, proportional to P. The oscillation frequency shift is very small (within 0.2 GHz) due to the small change of the reactive elements with power. This supports the fact that small-signal parameters can be used to predict the oscillation frequency accurately enough, as also shown experimentally by Maeda *et al.* [17]. A large-signal analysis is, however, needed for the prediction of the oscillator output power level and self-bias effects. Additional results of the large-signal analysis are presented in the next section together with measured characteristics.

IV. Large-Signal Analysis Results and Measured Oscillator Characteristics

The monolithic circuits were fabricated using the process described in Section II. A photograph of the D-band dual feedback oscillator is shown in Fig. 10. The chip size is 1.3 mm × 1.0 mm. At the end of the MMIC process, the wafer was thinned to 100 μm and diced into individual chips. The chips were then mounted in an in-house-developed test fixture for testing. The fixture has WR-5 waveguide ports and four bias lines. Care was taken to ensure a smooth surface for chip mounting, and a movable backshort was used for optimizing the waveguide-fixture transition characteristics. For the detection of the oscillation signal, the output of the test fixture was connected to a power meter through a frequency meter.

The gate bias was first fixed to the value necessary for maximum transconductance ($V_{gs} = -0.1$ V). The power and the dc drain current were then monitored as the drain bias was increased. The chip broke into oscillation at a V_{ds} of 1 V and a drain current decrease by 1 or 2 mA's was observed when the drain bias was raised from 0.9 to 1 V. This variation is believed due to self-biasing caused by the nonlinear gate-source junction conductance as the oscillation builds up. It is interesting to note that this current drop was much smaller than the one observed in lower fundamental frequency monolithic chips such as the Ka-band oscillators reported earlier by the authors [8]. The difference is apparently due to the shorting effect of gate-to-source capacitance, which is more pronounced at high frequencies. In order to verify this, D-band and Ka-band oscillators were simulated using large-signal analysis method, and the dc component of the drain oscillation current was evaluated as a function of the power delivered to the load. The results are shown in Fig. 11. The drain current change was much smaller at D-band (~3 mA) than at Ka-band (~10 mA). A similar trend was found in the dc component of the gate-to-source voltage (V_{gs}). The small dc current drop observed in the measurement is an indirect indication of fundamental signal generation.

The fundamental signal oscillation of the chip was found to be around 130 GHz. No external tuning was necessary for the circuit operation. The measured output frequency dependence on the gate and drain bias voltage is shown in Fig. 12. The oscillation frequency decreases with V_{gs} and increases with V_{ds}. This can be explained from the bias dependence of the HEMT equivalent circuit elements. In Fig. 13, the oscillation frequency (f_{osc}) has been calculated as the intrinsic equivalent circuit element values are varied up to approximately ±30 percent around the center value (at V_{gs} = maximum G_m point and V_{ds} = 1.1 V). The two capacitances, C_{gs} and C_{gd}, affect the oscillation frequency most. f_{osc} decreases monotonically

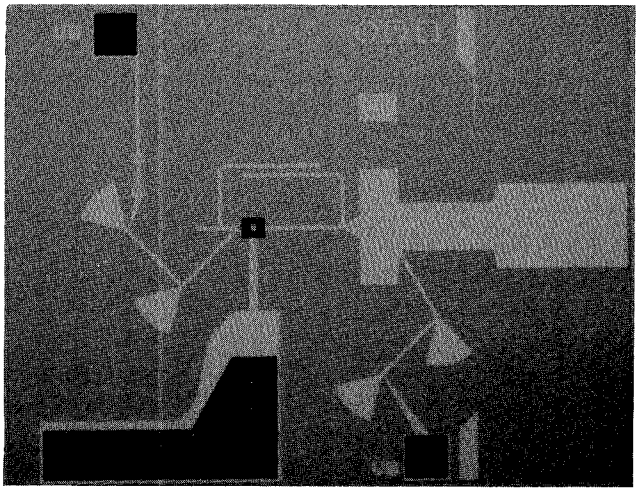

Fig. 10. Photograph of the D-band monolithic HEMT oscillator. The chip size is 1.3 mm × 1.0 mm.

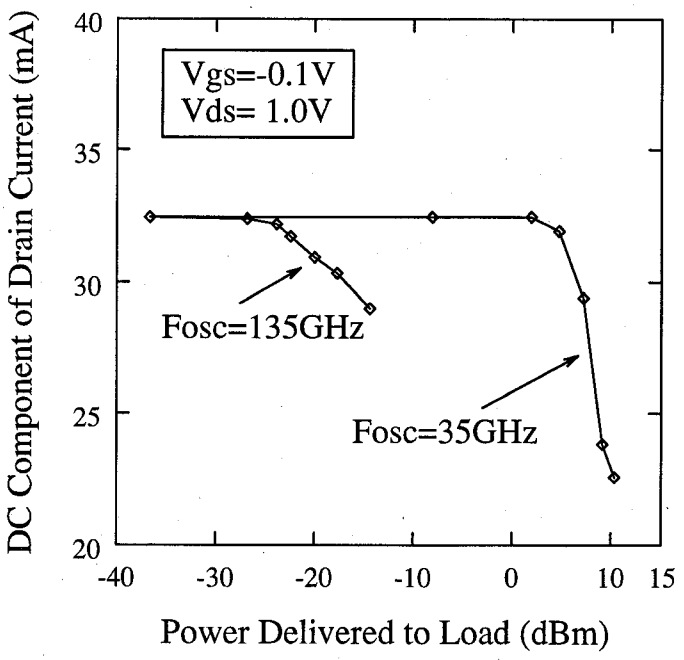

Fig. 11. Calculated dc component of the drain current as a function of the power delivered to load at two difference frequencies, illustrating the effect of self-bias.

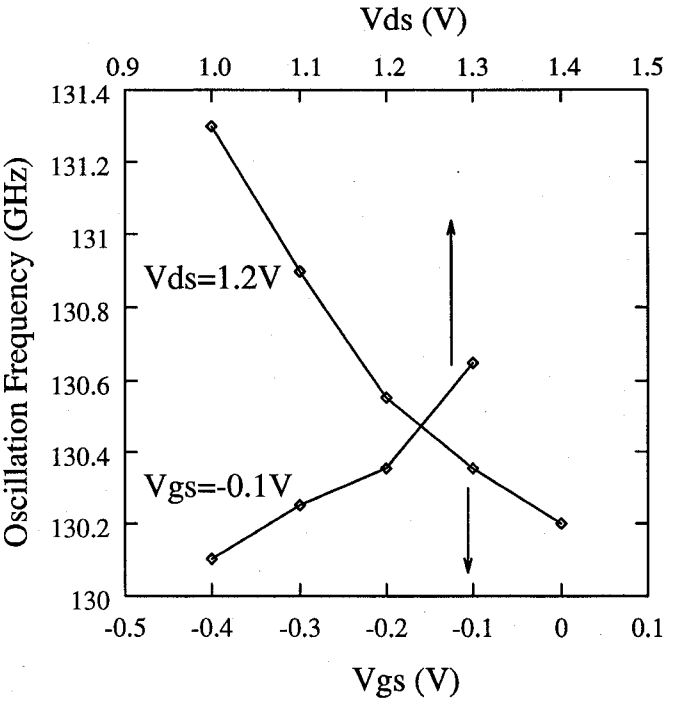

Fig. 12. Measured oscillation frequency as a function of V_{gs} and V_{ds}.

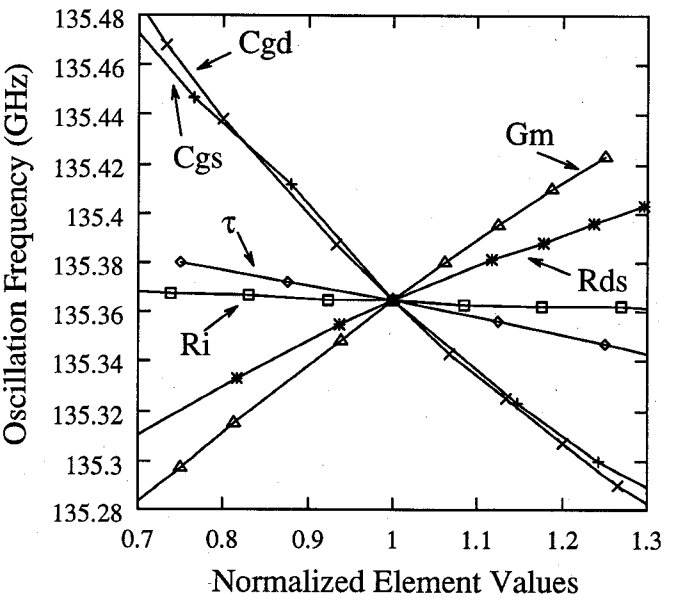

Fig. 13. Simulated oscillation frequency versus the intrinsic HEMT equivalent circuit element values which are varied up to ±30 percent around the center value.

with both capacitances as expected from the phase shift associated with them. G_m and R_{ds} also affect f_{osc} but a lesser degree. f_{osc} increases with both parameters. R_i and τ have very little impact on f_{osc}. The decrease of f_{osc} with V_{gs} is likely to be caused by the simultaneous increase of C_{gs} and C_{gd}, while variation of G_m and R_{ds} has a secondary effect. The measured gate bias tuning sensitivity was about −2.3 GHz/V. The oscillation frequency increase with V_{ds} can be explained by C_{gd} decrease and R_{ds} increase. C_{gs} increases with V_{ds} but the rate of increase is less than that of C_{gd} decrease. For example, C_{gs} increases from 105 to 125 fF (~19 percent change), and C_{gd} decreases from 15.1 to 9.8 fF (~35 percent change), as V_{ds} is increased from 1.1 to 1.6 V. On the other hand, R_{ds} increases monotonically with V_{ds} while G_m is not affected by V_{ds}, once V_{ds} is greater than the knee voltage. The drain bias tuning sensitivity should, however, be lower than the gate bias tuning sensitivity because of the compensation effect of C_{gs}. The measured drain bias tuning sensitivity was 1.67 GHz/V.

The measured and calculated oscillation power dependence on the gate bias voltage of the HEMT is shown in Fig. 14. The measured oscillation power varied by no more than 2 dBm over the gate voltage range of −0.3–0.0 V, which can be used as the tuning range. The calculated oscillation power was within 3 dB of the measured

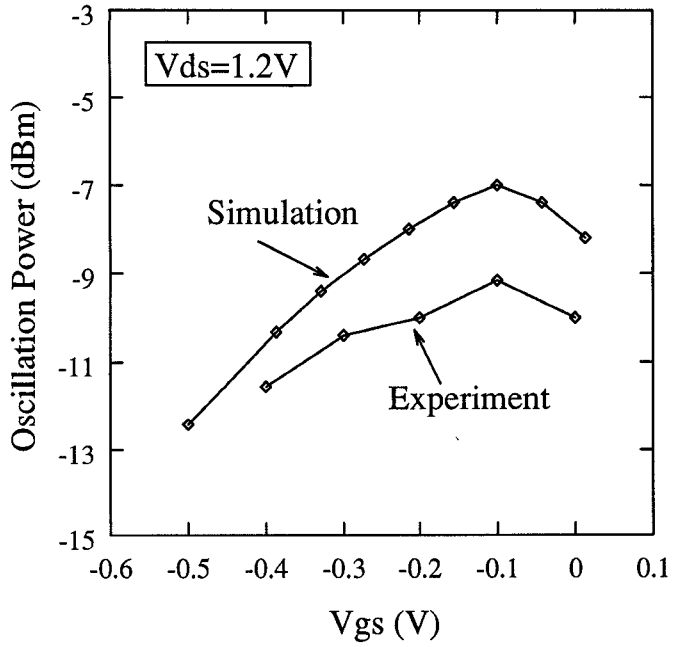

Fig. 14. Comparison of measured and simulated oscillation power at various V_{gs}.

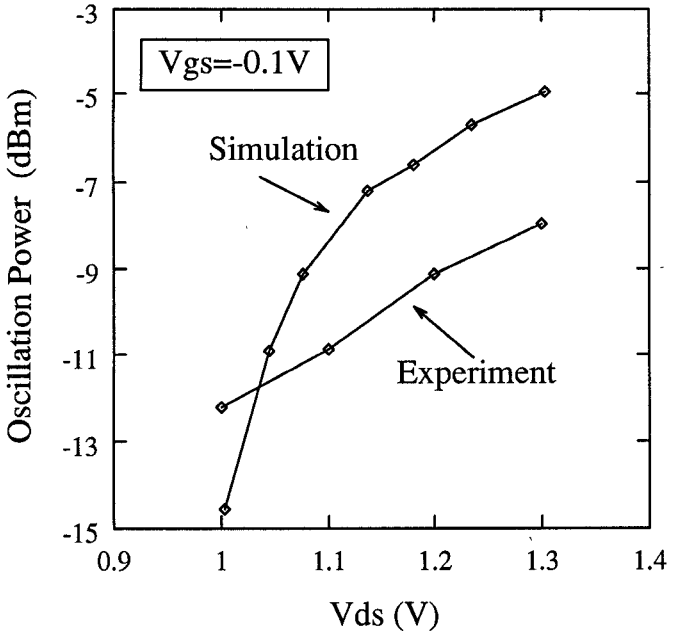

Fig. 15. Comparison of measured and simulated oscillation power at various V_{ds}.

data. This demonstrates the accuracy of the extracted parameters and the validity of our nonlinear modeling. The measured output power dependence on the drain bias voltage is compared with the simulation in Fig. 15. Simulated power is about 2–3 dB higher than the measured data, probably due to unaccounted losses from the transition and passive components. However, good overall agreement can again be found. While the oscillation frequency increases slightly with the drain bias, the oscillation power is found to be a strong function of drain bias voltage and increased from -12.2 to -7.9 dBm as V_{ds} varied from 1.0 to 1.3 V. This is related to the power gain improvement as the G_m/G_{ds} and C_{gs}/C_{gd} ratios increase with V_{ds}. The power level obtained from the chip was consistent with the small gate width (2 fingers of 0.1 μm $\times$ 45 μm) and low V_{ds} bias operation of the employed devices.

V. Conclusion

The first monolithic fundamental FET oscillator at D-band is demonstrated using submicron pseudomorphic DH-InAlAs/InGaAs HEMT technology. The circuit design was based on accurate HEMT modeling based on multibias S-parameter characterization. A special extraction method has been used for the evaluation of R_i and τ, which play an important role for the high-frequency modeling of the devices. The circuit uses dual feedback topology for enhanced negative resistance at D-band. The monolithic chip contained on-chip bias circuitry and an integrated E-field probe for direct signal radiation into a waveguide. The monolithic chip oscillated at 130.7 GHz with an output power of -7.9 dBm at the drain voltage of 1.3 V using 90 μm gate periphery HEMT's. In addition to the small-signal analysis, a large-signal analysis has been performed to investigate the nonlinear properties of the HEMT oscillators. The steady-state oscillation frequency was found to be close to the small-signal oscillation frequency, and the simulated output power levels were in good agreement with the measurement. This is the highest fundamental frequency signal generation reported out of monolithic chips using three-terminal devices, and demonstrates that InP-based HEMT MIMIC's are promising candidates for monolithic signal sources above 100 GHz.

Acknowledgment

The authors would like to thank P. Marsh for the test fixture and measurement support, Dr. G. I. Ng for valuable discussions about layer design and process technology, and K. Hong for wafer thinning.

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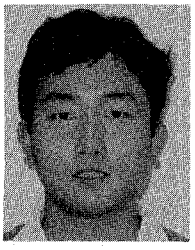

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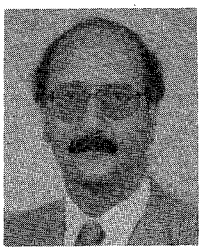

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Dwight C. Streit (S'81–M'86–SM'92) for a photograph and biography, see this issue p. 2302.